CSE 566 – Fall 2004
Reconfigurable System On Chip Design

Lecture 9 : COREs :
Logic Cores, Alliance Cores, and OpenCores.org

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Introduction to Cores

- A *core* is a ready-made function that you can instantiate into your design as a "black box"
- Cores can range in complexity
  - Simple arithmetic operators, such as adders, accumulators, and multipliers
  - System-level building blocks, including filters, transforms, and memories
  - Specialized functions, such as bus interfaces, controllers, and microprocessors
- Some cores can be customized with parameters

Benefits of Using Cores

- Save design time
  - Cores are created by expert designers who have in-depth knowledge of Xilinx FPGA architecture
  - Guaranteed functionality saves time for system verification
- Increase design performance
  - Cores that contain mapping and placement information have predictable performance
  - The data sheet for each core provides performance expectations

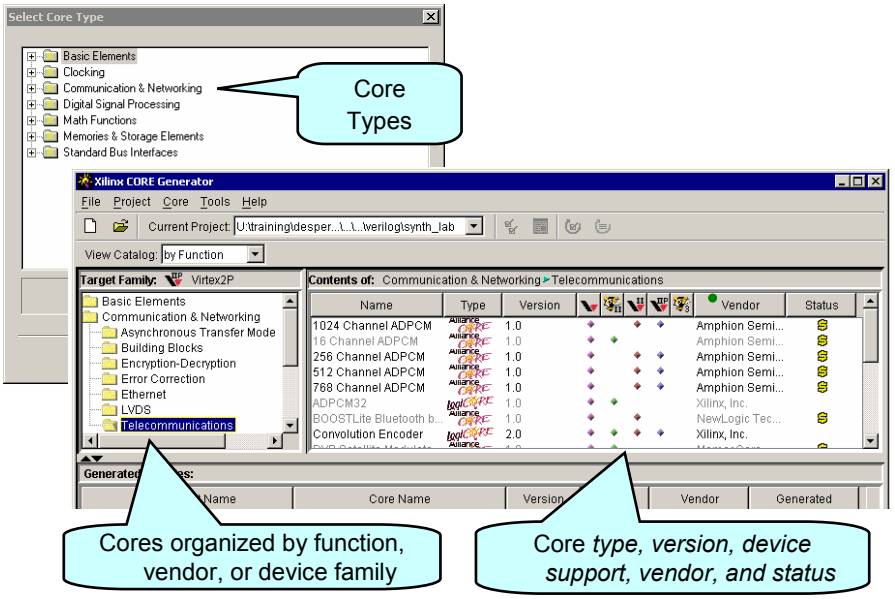
Available Cores

- LogiCORE™ solutions (Free)
  - DSP functions
    - Time skew buffers, FIR filters, correlators
  - Math functions
    - Accumulators, adders, multipliers, integrators, square root
  - Memories
    - Pipelined delay elements, single and dual-port RAM
    - Synchronous FIFOs
  - PCI master and slave interfaces, PCI bridge
- AllianceCORE™ solutions (Not Free)
  - Peripherals
    - DMA controllers
    - Programmable interrupt controllers
    - UARTs
  - Communications and networking
    - ATM
    - Reed-Solomon encoders / decoders
    - T1 framers
  - Standard bus interfaces
    - PCMCIA, USB

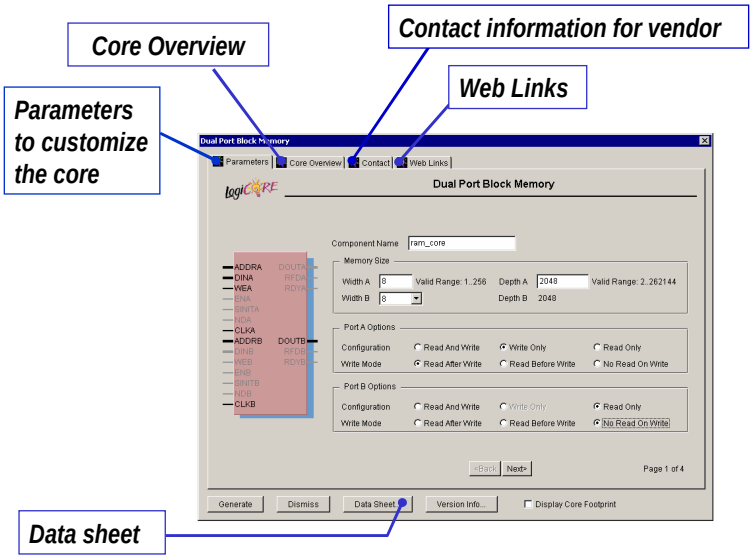
CORE Generator System

- Graphical User Interface (GUI) allows
  - Access to the cores themselves, with
  - Customizable parameters (available for some cores)
  - Data sheets
- Interfaces with design entry tools
  - Creates graphical symbols for schematic designs
  - Creates instantiation templates for HDL designs
- Web access from the Help menu
  - IP Center contains new cores to download and install
    - Provides access to the latest cores
  - Direct access to
    - http://support.xilinx.com

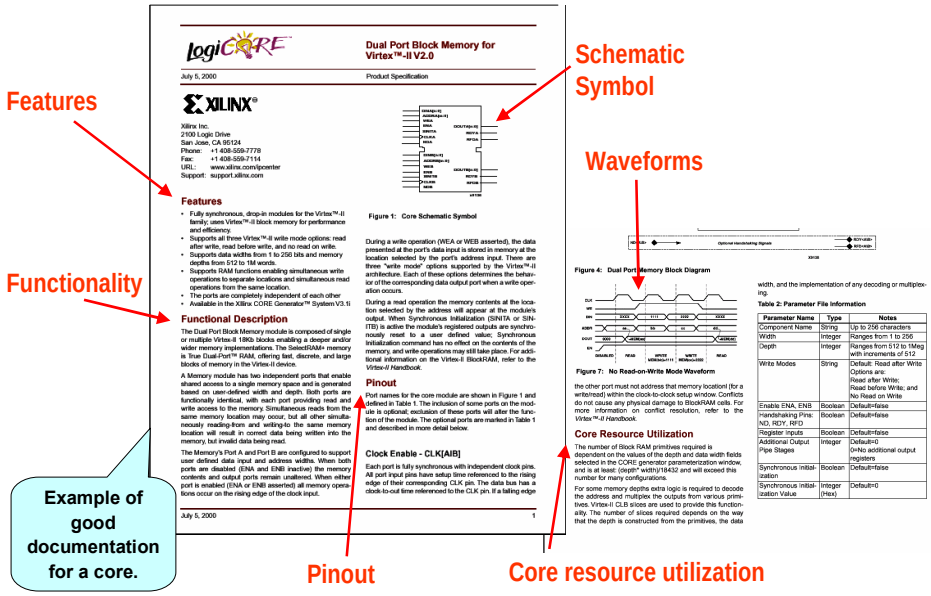
CORE Generator GUI



Customize cores with Parameters



Documentation : CORE Data Sheets



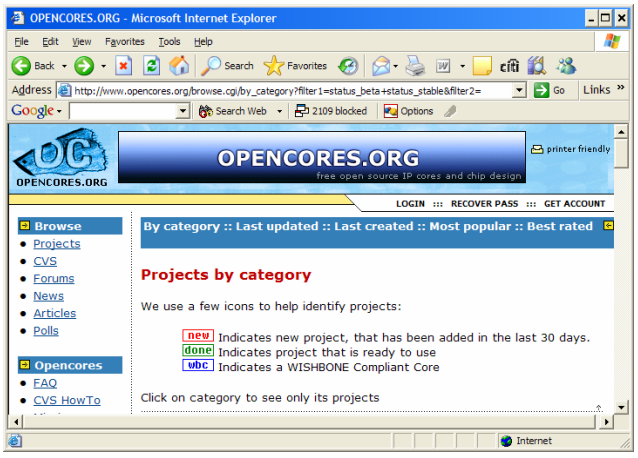
HDL Design Flow for Core Generation and Integration

- Generate core and produce:
  - Instantiation template files (VHO or VEO)
  - Netlist file (EDN)
  - Behavioral simulation wrapper files (VHD or V)
- Instantiate the core into your HDL source
  - Template provided in the VEO or VHO file
- Wrapper files enable behavioral simulation
  - Analyze the wrapper file for each core before analyzing the file that instantiates the core
- Synthesize and implement using Netlist (EDN)

Open Cores Website

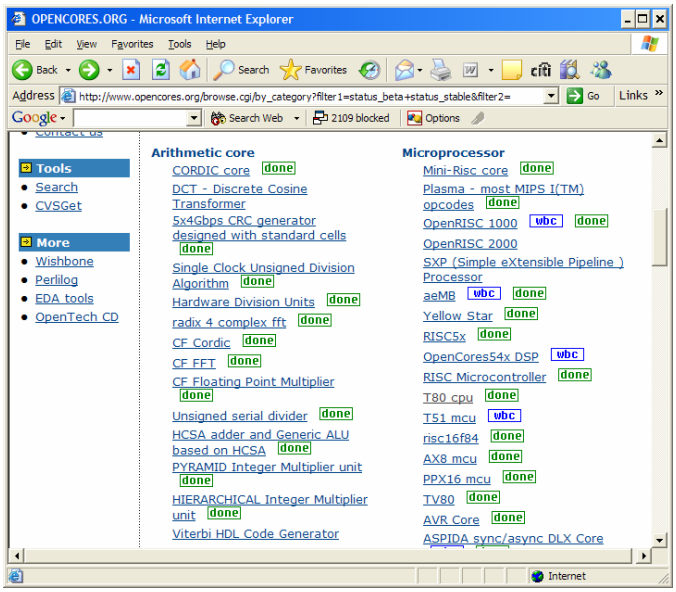
- OPENCORES.ORG
  - http://www.opencores.org/
  - Open souce cores in VHDL and Verilog source form
- Arithmetic
- Microprocessors
- Co-processors
- Communications
- Crypto
- DSP
- Memory
- AMBA bus

…



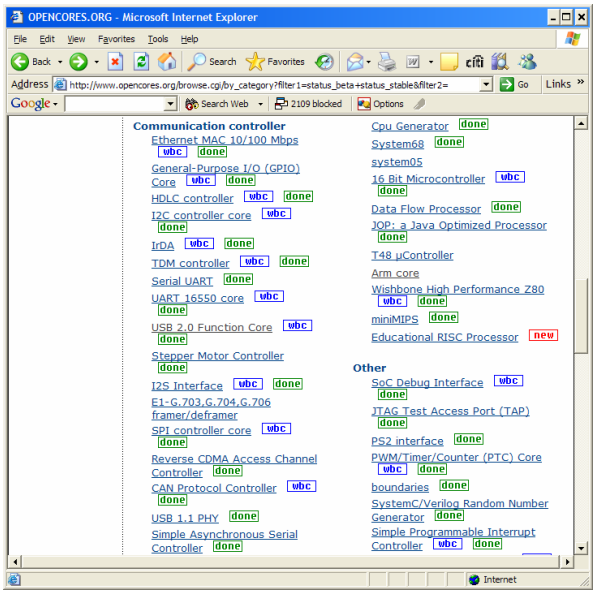
Open Arithmetic & Microprocessor Cores

- Arithmetic
  - Dividers
  - CRC
  - FFT
  - …
- Micro-processors
  - RISC
  - Z80
  - 32-bit
  - 16-bit
  - ARM
  - miniMIPS
  - …



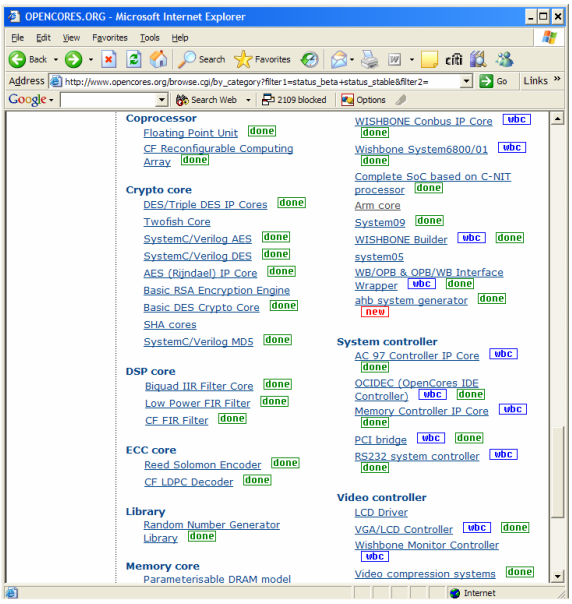
Open Communication Controllers Cores

- Communications
  - Ethernet 10/100 Mbps
  - HDLC
  - UART
  - USB 2.0
  - …
- Other
  - Random number generator
  - Interrupt controllers
  - …



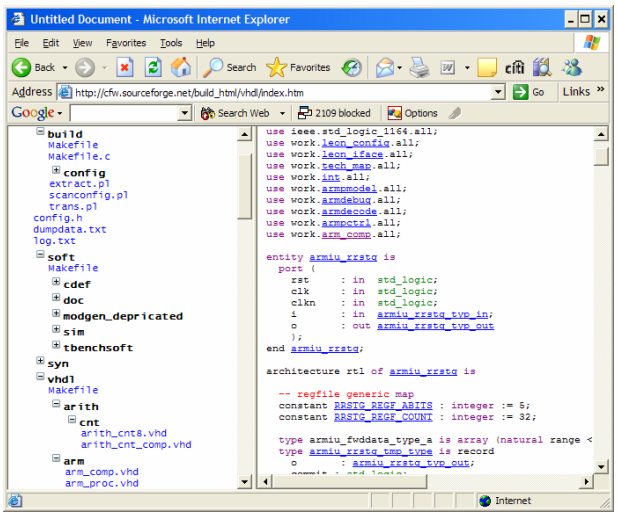
Open Crypto and Controller Cores

- Cryptography
  - DES/3DES
  - AES …
- Bus Controllers
  - Wishbone
  - AHB …
- Memory Controllers
  - SDRAM
  - DDR …
- System Controllers
  - PCI



Annotated VHDL source on SourceForge

- Open source ARM VHDL model
  - http://cfw.sourceforge.net/build_html/vhdl/index.htm
- Website provides access to VHDL source code
  - Color coded syntax
  - Hyperlinks



Washington University FPX Cores

- Layered Internet Protocol Wrappers
  - Process packets directly in hardware at Gigabit/second rates
- TCP/IP Protocol processing wrappers
  - Process millions of traffic flows in hardware at Gigabit/second rates
- Bloom filters
  - Find thousands of strings anywhere in data
  - Find longest matching prefixes of packets
- FP-Grep & FP-Sed
  - Search for Regular Expressions with wildcards
- Internet Worm Detection
  - Find malware passing through a network
- Switching and routing cores
  - Route traffic between FPGA components
- More information
  http://www.arl.wustl.edu/arl/projects/fpx/reconfig.htm

License Requirements for Cores

- Commercial Cores
  - Integrators pay to use the core (per core or per copy)
  - Authors receive royalty for use of core
- BSD-style license
  - No warranty
  - May be distributed in binary or source form
  - Authors must be acknowledged
- GNU Public License (GPL)
  - All modifications must be distributed under the GPL
  - Cannot take away rights to access a modified version of core
  - If you use an item under GPL item, you MUST distribute all information about it and NOT prevent others from redistributing or modifying it.
- Washington University FPX cores
  - Free for non-commercial use (i.e., university research)
  - License required for commercial use (i.e., product sales)
- Other licenses
  - Depend on the terms set by the author(s)